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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,343	11/18/2003	Schuyler E. Shimanek	X-1414 US	8186

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/717,343	SHIMANEK ET AL.
	Examiner	Art Unit
	Vibol Tan	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-17 and 22-28* is/are rejected.

7)☒ Claim(s) *5-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 12-17, 22 and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U. S. PAT. 5,487,037).

In claim 1, Lee teaches all claimed features in Fig. 11, a memory array comprising: a bitline (C); and a plurality of memory cells (RAM/ROM hybrid cells, abs.), each of the plurality of memory cells having: a configuration bit terminal (not shown but would be an output line coupled to an input of 1110, inherent); a pair of cross-coupled inverters (1110) having first and second bit nodes (cross-coupled nodes, not marked), wherein one of the first and second bit nodes is connected to the configuration bit terminal (not shown but would be the output line coupled to the input of 1110, inherent); an access transistor (1120) having a first current-carrying terminal (drain terminal) connected to the bitline, a second current-carrying terminal (source terminal) connected to the first bit node, and an access-transistor control terminal (gate terminal coupled to ROW); and a memory transistor (1140) having a first current-carrying terminal (drain) connected to one of the first and second bit nodes, a second current-carrying terminal

(source terminal) connected to a power supply node (ground), and a memory-transistor control terminal (gate terminal coupled to RE).

In claim 2, Lee further teaches the memory array of claim 1, further comprising a second configuration bit terminal (would be a second output line coupled to an output of 1110, inherent) connected to the first bit node, wherein the first- mentioned configuration bit terminal connects to the second bit node.

In claim 4, Lee further teaches the memory array of claim 1, the access-transistor control terminal receiving at least one of a read control signal and a write control signal (ROW).

In claims 12-14, Lee further teaches the memory array of claim 1, wherein the cross-coupled pair of inverters (1110s) is part of a static random-access memory (SRAM) cell (abs.); wherein the memory transistor is part of a read-only memory (ROM) cell (abs.); and wherein the memory array is part of a configuration memory of a programmable logic device (title).

In claim 15, Lee further teaches the memory array of claim 1 comprising a memory control terminal (a gate terminal of 1140 coupled to the gate terminal of the other 1140) connected to the memory transistor control terminals, the memory control terminal having first (RE is 1) and second (RE is 0) states, wherein the first state configures the memory cells as read-only memory (col. 10, line 12) and the second state configures the memory cells as random-access memory (col. 10, line 8).

In claim 16, Lee further teaches the memory array of claim 15, wherein the circuit is part of a configuration memory of a programmable logic device, and wherein the first

state of the memory control terminal (when RE 1) renders the programmable logic device an application specific circuit (ASIC).

In claim 17, Lee further teaches the memory array of claim 1, wherein the power supply node is ground (as shown).

Claims 22, 24 and 25 correspond to detailed circuitry already discussed similarly with regard to claims 1, 12 and 13.

Claims 26-28 correspond to detailed circuitry already discussed similarly with regard to claims 1, 12 and 13.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Zhang et al (U. S. PAT. 5,986,923).

In claim 3, Lee teaches the memory array of claim 1, with the exception of teaching a configurable resource connected to the configuration bit terminal, the configuration terminal transmitting a configuration voltage to the configurable resource. However, Zhang et al. teaches in Figs. 1 and 2, a configurable resource (I/O ports 112, 114) connected to the configuration bit terminal (D1' or D1), the configuration terminal

transmitting a configuration voltage to the configurable resource (col. 3, lines 1-3 and 58-60).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Lee with the teachings of Zhang et al. to force the configurable resource, I/O ports in Zhang, to the selected logic voltages, which are maintained as long as power is supplied to the memory cell, or until the memory is rewritten.

Claim 23 corresponds to detailed circuitry already discussed similarly with regard to claim 3.

5. Claims 5-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER